

# **EE 492 WEEKLY REPORT 8**

## **Project title: Fast, Compact, High, Strength, Magnetic Pulse Generator**

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Team Leader: Wei Shen Theh

Team Webmaster: Wing Yi Lwe

Team Communication Leaders: Jia yu Hong

Key Concept Holder: Aqila-Sarah Zulkifli

## Weekly Summary

For this week, we will continue working on SPICE simulation models. We will attempt to create and import a model if the SPICE model is still not made available to the team. On the other hand, new layout designs, which is the bare bone version of our design, were made as a constant board. We are looking to test if the safety feature we added are affecting the performance of the board and if the drawbacks are worthy trade-offs. This week will also be the second test on the working prototype.

## Past week accomplishments

Wei Shen received reply from TI. Unfortunately, they did not have that spice file, but they recommend some similar chips that had spice file. Since we have specified input capacitance requirement, we cannot use these similar chips (with high input capacitance). We know Multisim spice can edit parameters by using similar components. Wing Yi tried to import similar one, somehow she could not run these similar components in Multisim. When we tried to read the component library files in notepad, we could not understand because they were high level of software language. Wei Shen contacted TI again to request the spice file. Since We had problems to make DC input ground closed to pulse input and output grounds, so we decided to make fifth version of PCB by removing protecting circuits parts. Jiayu started to arrange fourth version. On Friday, Wing Yi and Aqila measured second testing for second version board, but they could not get correct data. After an hour, Jiayu tried to test again, the circuit still did not work.

## Pending issues

We were not able to run simulation as we cannot find SPICE files for both FETs. We need to debug and have second measurement. Also, the new inductors were tested with the old board but the readings were unusual. More testing needs to be done.

## Individual contributions

<u>NAME</u>	<u>Individual Contributions</u>	<u>Hours this week</u>	<u>HOURS cumulative</u>
Wei Shen Theh	New layout designs, continue search for transistor SPICE file, contact transistor supplier regarding SPICE file, alternate method for SPICE import	4	90
Wing Yi Lwe	Trials to import spice models into Multisim instead of Cadence Pspice, trials to test new inductors, attended group-advisor meetings, weekly report	4	75
Jiayu Hong	Worked on fourth PCB layout, measure the second version circuit, made sure members contributed on the weekly report and submitted the report	5	87
Aqila-Sarah Zulkifli	Measured second testing for second version board, attended group-advisor meetings, weekly report	4	74

## Summary of weekly advisor meeting

We focused on importing the models and tried different resources (such as National Instruments) online that could help us. Since sensing is expensive, so we discussed with our advisor. Our advisor told us that there were documentations on another current sensing resistor that we will investigate more on whether it is worth the change.

## Plan for coming week

Our plan for this coming week is to keep looking for the SPICE file for both chips and if we managed to find the files, we will be starting our simulation as soon as possible. Besides, Wing Yi and Aqila will try again on the measurement since last time we didn't get the results that we should get. We will also start planning on our poster design so that we won't be in rush. Other than that, we will be having our regular meeting on Wednesday at 3:30 PM and hopefully our advisors could join us this time so that we can have more ideas on how to fixed our problems.